GENERAL ELECTRIC
GENERAL ELECTRIC INFORMATION SYSTEMS ITALIA

GE 115/3 - 120 - 130
CONSOLE SUBSYSTEM

CROSS REFERENCE

This publication is composed of 2 volumes termed as follows :

Volume 1 T.o.C. 4.571.2.102. 2

- Description
- Installation)
- Maintenance) See C.P.U.
- Parts)

Volume 2F T.o.C. 4.571.2.103. 1

- Subsystem
- Schematics

Product composition by single unit and manufacturing level:

4.040.0.701. ☐

6.4.1970

GENERAL ELECTRIC
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GE 115/3 - 120 - 130
SOTTOSISTEMA CONSOLE

INDICE DI RIFERIMENTO

Questa pubblicazione è valida per i prodotti aventi i seguenti codici :
. 0897218 T.

Questa pubblicazione è costituita da 2 volumi definiti come di seguito :

Volume 1 indice 4.571.2.102.2

Descrizione
Installazione
Manutenzione } Vedi Unità Centrale
Catalogo

Volume 2F indice 4.571.2.103.1

Sottosistema
Schemi

Scheda anagrafica di prodotto:

4.040.0.701. ☐

6.4.1970

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GE 115/3 - 120 - 130
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This volume is applicable for those products having the following product codes: .0897218 T.

Binder 1 ", 3 rings

Window

Cross reference 4.571.2.101.2

T.o.C. 4.571.2.102.2

Description

1 Console subsystem - Description 4.571.1.201. /A
2 VAR 380 A 30004126.

6.4.1970

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GE 115/3 - 120 - 130
SOTTOSISTEMA CONSOLE

INDICE DEL VOLUME 1

Questo volume è valido per i prodotti aventi i seguenti codici :
. 0897218 T.

Raccoglitore da 1", a 3 anelli

Finestra

Indice di riferimento 4.571.2.101. 2

Indice 4.571.2.102.2

Descrizione

1 Sottosistema Console - Descrizione 4.571.1.201.

2 VAR 380 A - Prova piastre 30004126.

5.1.1970

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GE 130

CONSOLE SUBSYSTEM

Description

A Field Engineering
publication

4.571.1.201.0/A

REVISION LEVEL

UPDATE Nº	PAGES AFFECTED	DATE
	First edition - Title page P.N. 4.571.1.201.0/A	January 1969

Mod. 0752

N.B. Remove pages identified with crossed numbers

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1. GENERAL CHARACTERISTICS

The console, or Wing F, consists of the following Elementary Units.

TAV 460 A - Operator Panel and Maintenance Panel.
CON 460 A - Console cabinet.
VAR 380 A - Board Tester.
VAR 450 A - Fan Power Supply distribution and control.
TAV 421 C - Remote control rig.
VAR 360 B - Elapsed time counter (optional)

- Description of the TAV 460 can be found in the GE 130 CPU description manual (PDS cod. 30004122).
- Description of the TAV 421 C can also be found in the above mentioned manual.

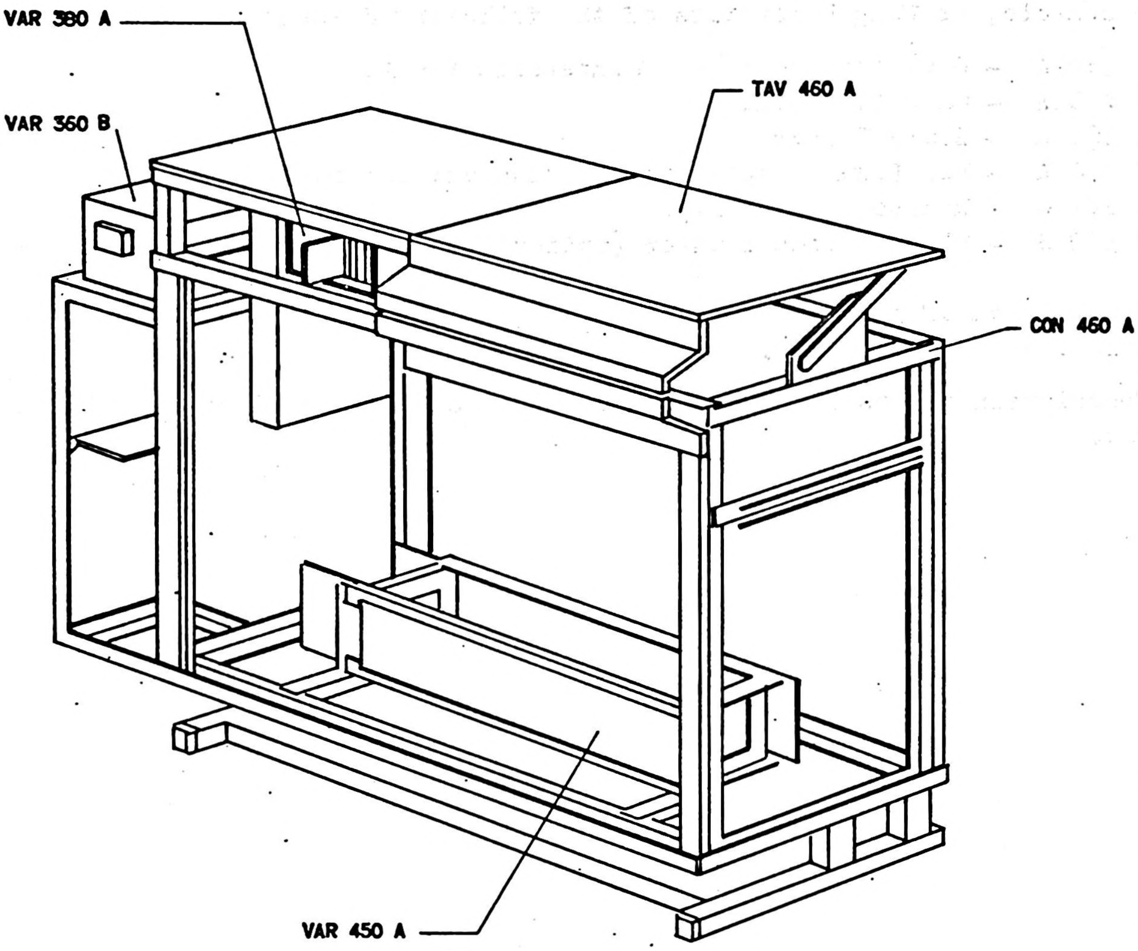

Fig. 1.1. - Console Subsystem

2. VAR450A

This unit, used for the fan power supply distribution and control, has a size equal to that of half an SMN module and is positioned on the console cabinet base.

Fixed to the front hinged panel are the terminal strips, running parallel with each other. The first one is connected to Power Supply wing as follows:

- terminals 1 through 5 - to the ALI 032 P2 terminal strip (fan power supply),
- terminals 7 through 9 - to the VAR 300 P1 terminal strip (fan control).

The remaining 5 terminal strips are used to connect up other fan groups of the various subsystems within the system itself.

P.D.S.
Board-tester device - VAR 380
1° APPLIC.

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Cod. 3696128 F

1. General

1.1. The board tester device (VAR 380), described here, is used to detect the faulty component on the boards, done with the SCM 3 standard.

This device is located in the console cabinet of the GE 130.

1.2. Composing parts and application procedures

1.2.1. The main parts forming the board tester are:

a) complete set of cards corresponding to the boards which may be tested and relative container;

b) automatic card reader;

c) storage and comparison logic circuits;

d) operating panel.

1.2.2. Application procedures.
Detailed indications of the application procedure are specified in para. 4.2. and in the CPU documentation - Volume V.

1.3. Application field

Suitable diagnostic programs will detect the board or the boards which may be assumed as faulty.

The type of boards of the GE 130 which can be tested is given in the introduction of the FAULT vocabulary.

The present device may be used also to test the boards belonging to controllers realized with the SCM 3 standard.

2. Composing parts description

2.1. Cards and reader

The cards to be used to test the boards are made with aluminum alloy: the "1" or the "0" correspond to whether there is or not a semispheric drawing of a diameter of about 2 mm. There is a card for every board to be tested; there are 2 cards for one board only exceptionally. A card has a maximum of 21 rows and every row consists of 30 bits ("1" or "0").

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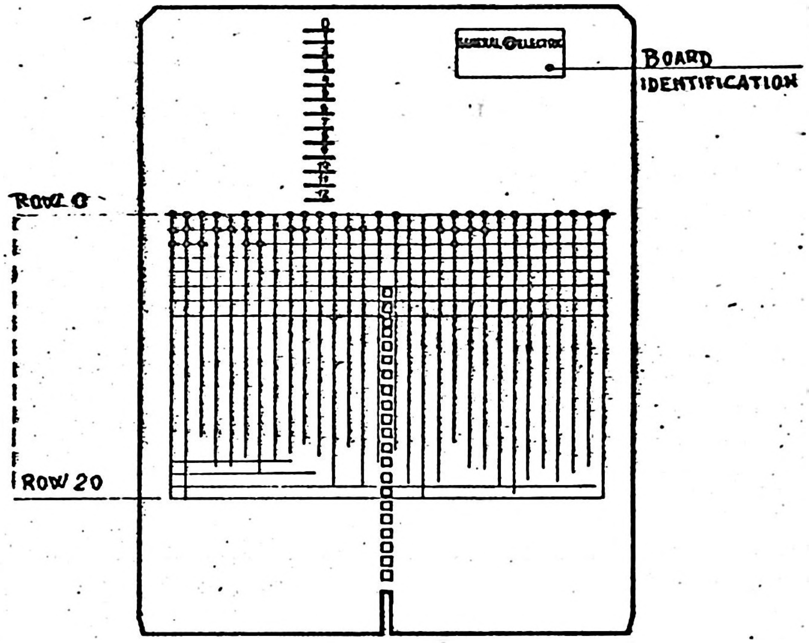

Row "0" contains the information necessary to recognize the pins of input and output from the board under test; the following rows (1 to 20) contain the information concerning the test configuration.

The card movement in the reader is done automatically, by means of a bar kept in pressure by two springs.
The positioning of the card with respect to the reader, in the moment in which a row is read, is obtained by means of a system with a double ratchet gear.
At the center of the card there is suitable numbering which allows to recognize the number of the test under way.
There is another writing on the card which allows the identification of the board to which the card refers.
The reader consists of a series of 30 test-points.
These test points have electric contacts which in rest position are normally closed and energized with current (logic "0").
When a test-point is positioned on a semi-spheric drawn zone of the card, the contact opens showing at its terminals a positive voltage (logic "1"); the 30 electric signals ("0" and "1") which are obtained in correspondence of one row are then stored in the FF of the board tester at the pressure of the reading push-button (START).

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2.2. Logic circuits

The logic circuits are used to store the information arriving from the reader, to send logic signals to the inputs of the boards under test, to compare the outputs of the board with the signals which represent the correct output for the considered input configuration; should the comparison give a negative result, the panel check lamps turn on.
The same logic circuits allow the identification of the pins of input and output of the boards under test and the correct positioning of the panel switches.

2.3. Standard used

2.3.1. Circuits

The logic of the board tester consists of integrated circuits belonging to the SCM 3 standard used for the GE 130 and for the controllers.
In particular, AND-OR-Inverter and 2 or 3 input NAND's of the TTL family.
The monostables and the interface circuits consists of discrete components.

2.3.2. Components

In addition to the given integrated circuits, we have used transistors of the standard type (1W8907), 32 12V 20 mA lamps, resistors, standard capacitors, 31 two-way switches(the same type used on the 130 panel), one 3-way switch, one 1A 3AG fuse.

2.3.3. Media

Boards and SMN connectors are used.
11 boards with plated holes are used: 10 are repeatitive.
The total number of boards is 12 of which: 10 serve for the logic functions (FULO 2A), 1 for the commands (COMA 2A),1 to filter the power supply voltages (FILT 2B).

2.4. Insertion and power supply

2.4.1. Insertion

The board tester is inserted in the area to the left in the maintenance console cabinet of the GE 130 above the area reserved for the cables. The sizes of the board tester panel are 282 x 283 mm.
Both the reader and the logic boards are clamped to the board tester panel.

2.4.2. Power supply

The board tester needs 2 voltages (taken from the CPU power supply):

+5V absorption	1.7A	for the logic circuits
+12V absorption	0.7A	for the lamps

The board tester does not need any ventilation device.
The protection against the short-circuits of the +5V voltage towards ground is performed by the devices present in the CPU power supply.
A fuse of 1 Amp is in series with the +12V voltage in order to avoid that short-circuits between +12 and +5 cause failures of the circuits.
The Zener diodes set in parallel to the +5V assure that this voltage does not reach dangerous values, because of a short-circuit between +5 and +12, also during the transient, i.e. when the fuse is not yet interrupted.
A short-circuit between +12 and ground causes the intervention of the protection on the CPU +12 power supply and/or may cause the opening of the fuse.

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3. Functional description

3.1. General and definitions

The diagnosis of a board with failure detection at electronic component level (integrated circuits package or transistors)is done applying to the inputs of the connector of the logic network on the board a series of combination of logic levels and interpreting the signal of possible errors in the levels which show on the outputs brought back to connector of the network itself.

The following definitions are valid.

3.1.1. Test configuration

A test configuration is defined as a special combination of logic levels (logic 0 or 1) related to all the pins of the board. In correspondence with the input pins there are the logic levels forming the real diagnostic test; in correspondence to the output pins there are the correct levels consequent to the logic input levels.

The test configuration refers to the 30 pins used as logic signals (the 4 ground and power supply pins are not included). The arrangement of the pins in the test configuration repeats the topographic disposition of the connector pin.

3.1.2. Error configuration

An error configuration is defined as a special combination of control signals (lamp off or on) relative to all the pins of the board, at the moment of the application of a test configuration.

In particular, the control signal is significant only in correspondence with the output pins: in this case "Lamp off"("on") means correct (wrong) output level. In correspondence with the input pins there is always the signal "Lamp off".

The error configuration refers to the 30 pins of logic signal with the same arrangement of the pins on the connector.

3.1.3. Test execution

The testing of the board consists of a first phase of presetting of the connection of the pins of the board to the logic of the device, and of a second test configuration and of inspection of the corresponding error configuration.

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3.1.4. Presetting of the test

In this phase, we prepare the connection of the board input and output pins to the logic of the device, so that in correspondence with every test configuration the input pins receive the logic levels planned by the diagnostic program and the levels of the output pins are compared with the correct levels.

The unconnected pins (not used by the board logic) are treated as input pins.

The presetting of the test is done introducing the card in the board tester reader in the position of row "0" (on which there is the information concerning the arrangement of the input and output pins on the board connector)and suitably operating on the input and output switches according to the procedure specified further on.

3.1.5. Application of the test configuration

In this phase, the logic network contained in the board is tested, in sequence with suitable level configurations on the input pins, and from time to time, the real level of every output pin is compared with the correct level, giving out the related error signal.

The test configurations - precalculated with the methods of the diagnostics oriented towards the failure detection show the following characteristics:

a) for a reduced assembly of diagnostic programs suitable to cover all the steady failures which may occur in real malfunction situation;

b) they entail a diagnostic test of the static type of the network under exam, in the sense that electric levels constant for the whole application time of the individual test configuration are applied to the input pins of the board;

c) they follow a pre-arranged sequence. The order of this sequence - negligeable in the case of purely combinatorial networks - is essential in the diagnosis of networks with memory (networks containing flip-flops with or without sequential loops); in this last case, in addition, we have abolished the situation which may cause "critical races" in passing from one test configuration to the following.

The application of the test configuration sequence is obtained moving the card forward in the board-tester reader to the posi

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tion of rows 1,2,3...etc. in sequence, after having had a permission to read for every position (see para. 4.2.). It must be noted that the movement forward is significant only from the bottom to the top, for the correct application of the sequence of the test configurations.

3.1.6. Additional performances

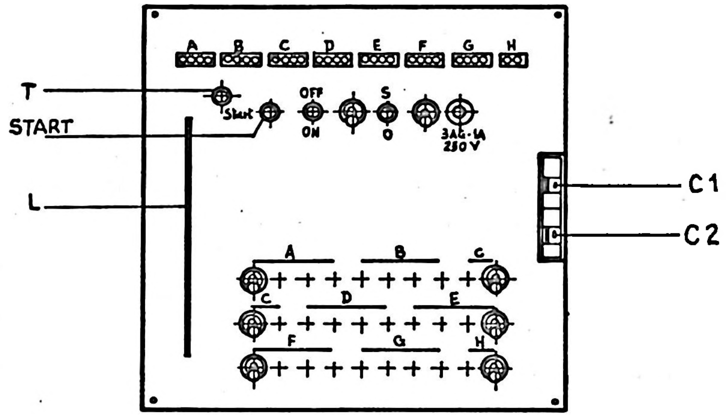
3.1.6.1. Protection from wrong operation.
The device is designed in such a way that a wrong operation does not cause failures either on the board under operation or the device itself.

3.1.6.2. Capacity for self-diagnosis.
The probability of a failure in the board-tester logic is very low with respect to the probability of a failure in the C.P.U. Nevertheless, a simple procedure to test the device (*) has been planned to insure the correct performance of the device itself and to allow to repair it, should it fail.

(*) refer to para. 4.2.5.

4. Operability characteristics

4.1. Panel description



The Board-Tester panel is given in the figure.
The panel consists of the following different parts:

4.1.1. Card reader - L -

It is sited in the left part of the console.
The card is inserted vertically in it, the forward movement occurs pressing the specific push-button.

4.1.2. Connector - C -

It is a double SMN connector within which the board to be tested must be inserted vertically.

4.1.3. Powering On - Powering Off

The ON-OFF switch serves to give to or to take away from the board-tester the power supply: it is in series with the +5V and +12V power supply and with the MAINT ON control signal arriving from C.P.U.
In the position ON the lamp L1 must be on.

4.1.4. Signals

In the upper part of the panel there are 30 check lamps aligned on one line and divided in 7 groups of 4 lamps each plus one group of 2 lamps and labelled with A (1,2,3,4), B (1,2,3,4), C (1,2,3,4), ... H (1,2); an input-output switch labelled with A1, A2, A3, ... H1, H2 corresponds to every lamp.

4.1.5. Operation switches

4.1.5.1. The switch O-S must be in position O when row "O" of the card is read, and in position S when the following rows are read.
The lamp L2 is lit when the switch is in position O, it is not lit when the switch is in position S.

4.1.5.2. The input-output switches A1, A2, A3, A4, B1, B2,.... H1, H2 are 30 as the check lamps and correspond to the 30 signal pins of the board under test.
When the switches are turned toward the top, they are in input position; when they are turned towards the bottom they are in output position.

4.1.5.3. START push-button. The START push-button enables the reading of one row of the card; it will have to be pressed only after the correct positioning of the card in correspondence of the row to be read is accomplished.

4.1.5.4. T push-button. It commands the movement forward of one test row.

4.2. Board tester operation procedure

4.2.1. Taking the boards out from the machine

The boards, that the diagnostic program has detected as probably faulty, must be taken out from the machine, when it is powered off.

4.2.2. Switches positioning

The O-S switch must be in position O.

4.2.3. Insertion on connector C of the board to be tested

4.2.4. Powering the board tester on

After the machine has been powered-on, turn the board tester on. Switch ON-OFF in position ON.

4.2.5. Board tester check

4.2.5.1. Switches A1, A2, ... H1, H2 must be set in output position (all toward the bottom).
The pressure of START must cause the switching on of all the check lamps.

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4.2.5.2. All the switches A1, A2, ... H1, H2 are then set in input position (all toward the top).
The pressure of START must turn off all the check lamps.

4.2.6. Input-output switches positioning

4.2.6.1. The card is inserted in the reader slot and is pressed to the bottom. Then row 0 is read pressing START.
This turns on some check lamps.
It is then necessary to set in output position the switches corresponding to the lamps lit.
Pressing START again, if the positioning of the switches was correct, all the lamps, should be not lit.

4.2.6.2. Once this operation has been accomplished the O-S switch is set in position S.

4.2.7. Board test

4.2.7.1. Pressing push-button T the card moves forward and row 1 is read pressing START.
If the lamps do not light, the card is moved to row 2 START is pressed again ...... etc.
The lighting of the lamps after the pressure of START means board not working.

4.2.7.2. It is then necessary to consult the FAULT vocabulary and from the number and the position of the lamps lit, for every test, it is possible to identify the faulty package.

4.2.8. Component replacement

4.2.8.1. Once the package to be replaced has been identified, switch O-S is moved to position O.
After the faulty package has been replaced with one working correctly, repeat the test from the beginning.
If the board has been repaired correctly, the check lamps in tests 1, 2, 3, ... n, after every pressure of START must stay unlit.

4.2.8.2. Should there be some indecision on several packages, replace one package at a time, and after every replacement, test the board again.

4.2.8.3. If the suspected circuit has discrete components, replace the transistor.

5. Performances related with the GE 130 C.P.U.

5.1. Circuits treated

The integrated circuits of the standard and some discrete components circuits may be tested.

5.1.1. Boards consisting only of integrated circuits

5.1.1.1. The board tester can test boards consisting of integrated circuits interconnected.
These circuits are the ones of the standard:

1) NAND with 2,3,4 and 8 inputs of the TTL family;
2) AND-OR-INVERTER with 4 inputs of the TTL family;
3) Flip-Flop in direct set-reset done with NAND and/or AND-OR-INVERTER of the TTL family;
4) Master Slave Flip-Flops done with NAND of the TTL family;
5) Master Slave Flip-Flop in one package only of the DTL family;
6) Flip-Flop "Latch" done with AND-OR-INVERTER and/or NAND of the TTL family.

5.1.1.2. Nevertheless it is necessary to comply with some general rules.

a) An input pin of a board cannot be connected with more than 9 or equivalent TTL loads.
b) A signal coming out from the board must not drive on that board more than 7 or equivalent TTL loads.
c) The ground and +5V power supply pins must occupy respectively positions 17 and 8 in the SMN connectors.

The boards of the GE 130 C.P.U. comply with these rules.
It is necessary to check that every new integrated circuit eventually added to the standard can be tested by the device.
This check will have to be performed by the Circuits Office.

5.1.2. Boards consisting of integrated circuits and discrete components circuits

The board tester is in the condition to examine boards with the following circuits: monostable, interface circuits, NOR circuits of memory.

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The boards containing filter and push - button circuits and lamps driving circuits (two different types), might need a procedure which is slightly different from the one given in para. 4.2.

5.1.2.1. Monostable

The treated monostable has a period of 1.2 us ± 15%.
The correct emission of the output pulse in function of the input signals is checked.
The period of the output pulse is not checked.
For the monostables which could be designed in the future, the following must be considered:

a) monostables with pulses with a period of $<$300 ns are not tested;
b) monostables with pulses with a period included between 300 and 900 ns may cause uncertainty in the board-tester answer;
c) monostables with pulses with a period above 900 ns are tested.

It must be noted that a board, which contains a monostable driving a Flip-Flop, may be tested, independently from the period of the pulse of the monostable.

5.1.2.2. Interface circuits

The interface circuits of the GE 130 may be tested, pointing out that, for the transmitting circuit, a possible opening of the Zener diode set on the output is not detected.
There are some board designing bonds (established in the standard application procedures) which must be complied with in designing new interface boards so that they can be tested with the board tester.

5.1.2.3. The NOR circuit of memory (which is set on the LOGI-MC board) may be examined by the board tester.

5.2. Boards tested

These boards can be divided in the three following groups according to the diagnostic point of view:

- boards which can be examined by the board-tester
- boards which can be examined with conventional means
- spare boards.

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5.2.1. Boards which can be examined by the board tester

They are double boards with SMN connector, containing integrated circuits and/or circuits of the type indicated sub point 5.1.2.

60 is the number of the different types (equal to 73% of the total types of boards).

These boards can still be divided in combinatorial boards and sequential boards.

5.2.1.1. Combinatorial boards (number of different types: 38). They are boards containing only combinatorial networks.

5.2.1.2. Sequential boards (number of different types: 22). They are boards containing Flip-Flops with or without sequential loops.

5.3. Test times

5.3.1. Mean test time of a board with no failures

This time includes only the operations of preparation and card movement up to the last test configuration. This time has been evaluated around 2 min.

5.3.2. Mean time to test and repair a faulty board

This time includes, besides the operations mentioned sub point 5.3.1., also the consulting of the FAULT vocabulary, the faulty component replacement and the check of the correct replacement. This time has been evaluated around 15 min. (10 min. for the repair).

5.3.3. Mean time of the intervention with the board tester

This time depends on the number of suspected boards given by the general diagnostic procedure. Referring to an incertitute of three boards, generally the intervention with the device will end at the second board; the time of this intervention is evaluated around 17 min. (as sum of the two previous periods, in case of replacement of one faulty component only).

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6. Circuitry description

6.1. Commands board (COMA 2A)

Refer to fig. no. 3.
Pressing START the FF COC01 (boxes 2 and 7) goes to reset, when released goes to set.
With the positive edge of the COCOA signal the two pulses MAS 11 and MAS 21 are obtained.
MAS 11 is a positive pulse lasting 100 ns which stores on the various FULO boards the information arriving from the row of the test card.
MAS 2A is a negative pulse of 800 ns which stores on the various FULO boards the result of the comparison between the stored signals arriving from the test card and those arriving from the pins of the board under test.

The signal LAOF1 supplies the ON/OFF lamp
The signal LAOSA supplies the O/S lamp
The ALP01 enables the switching on of the lamps during the exam of row 0 of the test card.

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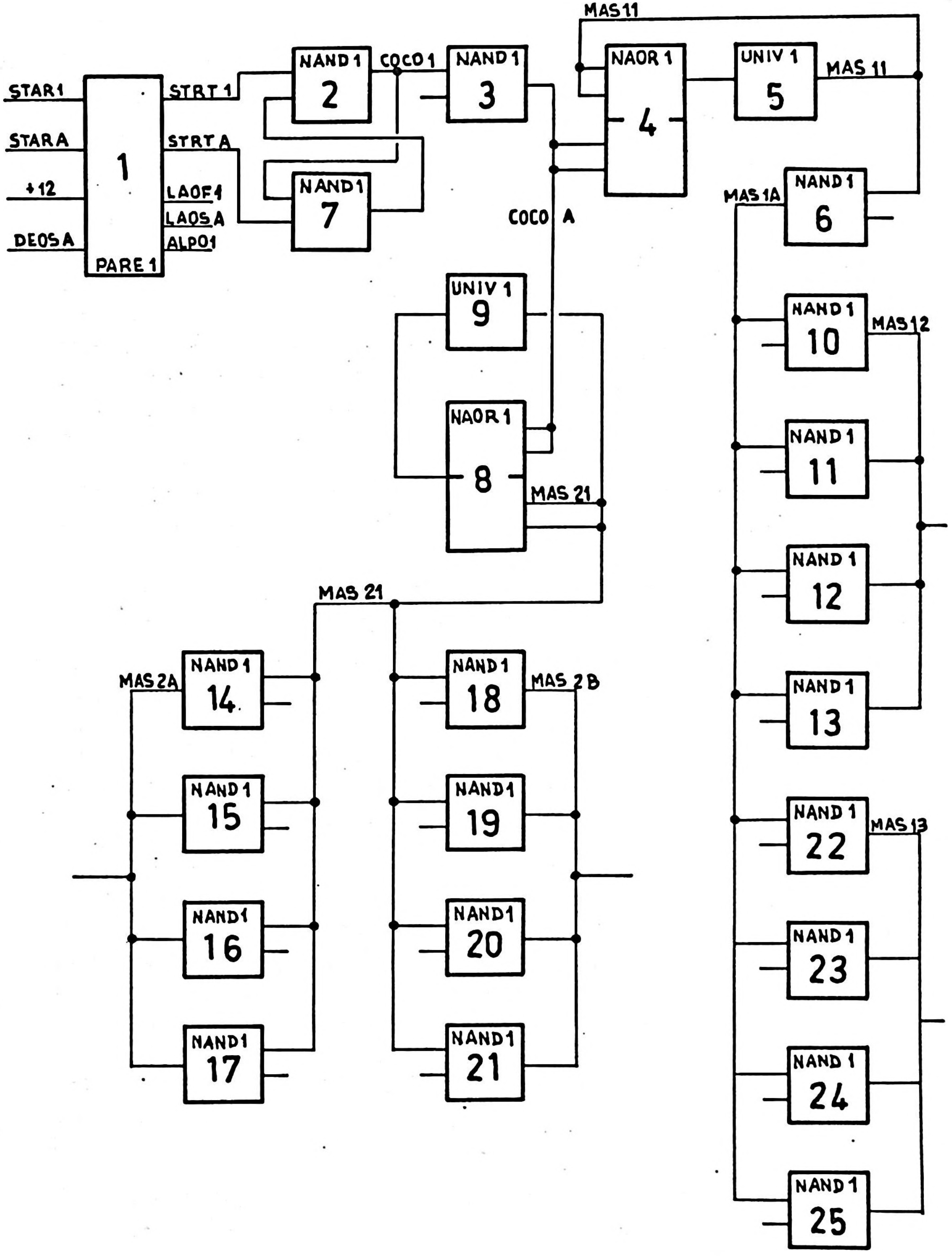

Fig. 3

Commands board

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6.2. Logic functions board (FULO 2A)

The circuit related to pin 1 of the board under exam is described (refer to figure 4).

FF SC011 (box 8) stores with the pulse MAS 13 the information arriving from the test card.
If there is the drawing, the signal LE011(6) is at "1" therefore the FF is set.
If there is no drawing, the FF is reset.
The signal thus stored is then sent to NAOR1 (box 9) which performs the comparison between the configuration arriving from the test card and the signal arriving from the output pin of the board under test.

The signal PT011(14) is the one arriving from the board pin and generates the signal IU011 which is sent for the comparison to NAOR(9).
The signal CO011 will be at "1" when the signal IU011 and SC011 are at a different logic level.

Should the pin under exam be an input pin, the inverted SC01A signal (USO 11) is short-circuited with the signal IU011(14) through the switch in input position.
In this way the signal IU011, beside being sent to the input pin, is formed in such a way that the comparison gives always the same result (CO01 = 0).

The FF CA011, when it is set, drives the switching of the lamp A1. During the performance of the test relative to row 0, the signal ALP01(1) is at "1". Being all the switches in output position, the signal SE011 is at "1". If the signal LE011 is at "1" it means that the pin must be considered as output.
ALP01. SE011. LE011 = 0, therefore FF CA011 goes to set and makes the lamp turn on.
Setting the switch A1 in output position, the signal SE011 goes to "0".
Pressing START CA011 goes to reset and the lamp turns off.

During the performance of the subsequent tests the signal ALP01 = 0 stops TE01A = 1.
The FF CA011 passes to set and will turn the lamp on only when at the arrival of the pulse MAS22 the output of the comparison NAOR CO011 will be equal to "1" i.e. when there will be a discrepancy between the signals arriving from the test card and from the board under test.

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The above described performance is valid for all the 30 circuits related to the 30 pins of the board under test.

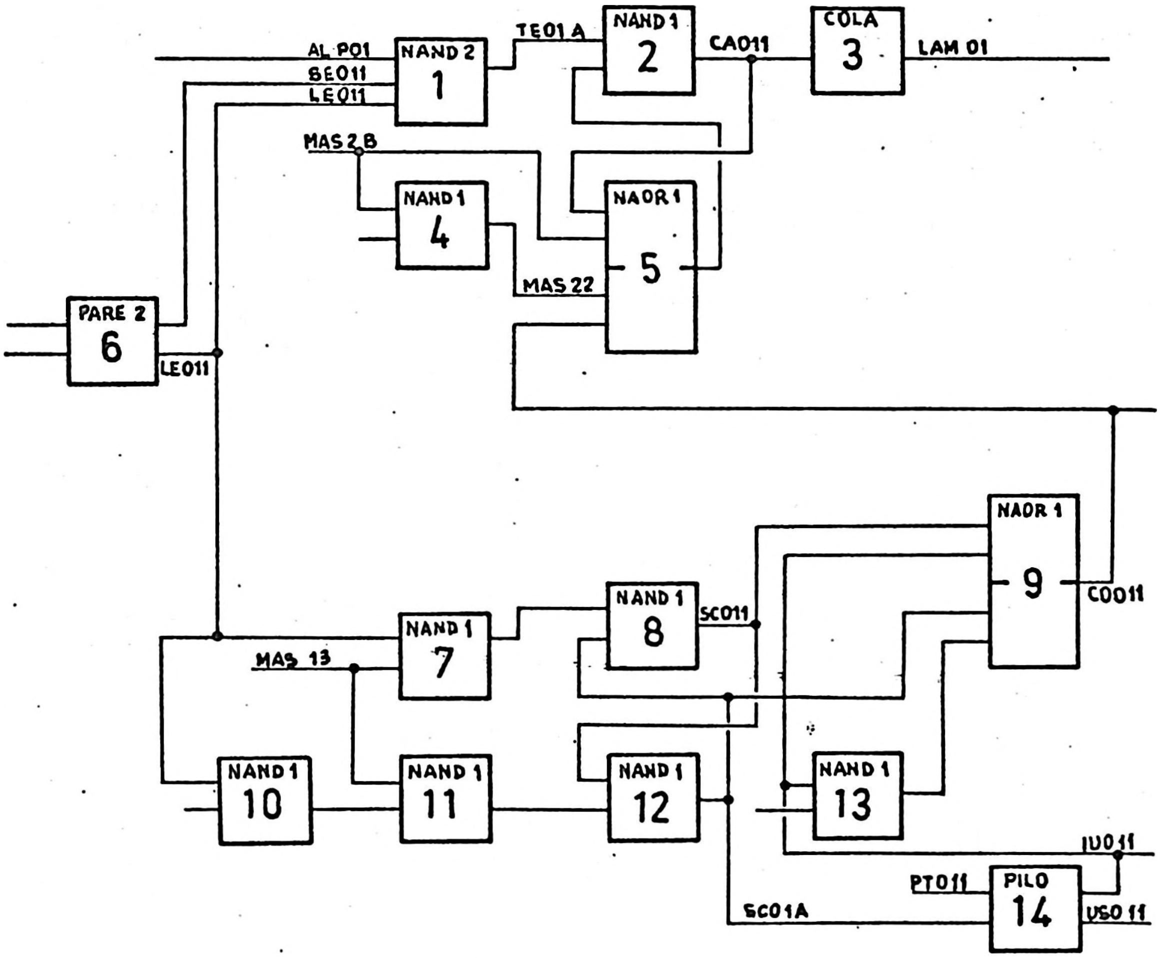

Fig. 4

Boards (logic functions)
(signals related to the 1st pin)